CLAIMS

1. A semiconductor structure formed by a method comprising:

forming a first layer on a surface of a silicon substrate having a first thickness;

forming an opening having a first width through the layer;

forming a blanket dielectric layer having a second thickness on the first layer and in the opening, the second thickness being less than the first thickness;

removing the blanket dielectric layer from the layer and bottom of the opening, but not from sidewalls of the opening, to form dielectric spacers on each side wall within the opening, the gap having a second width less than the first width;

implanting ions into the substrate at a location beneath at least one of the dielectric spacers, the implanting being performed at an angle to provide implanted ions under the at least one dielectric spacer;

depositing a gate electrode into the gap after implanting ions through the gap;

removing the first layer and leaving the dielectric spacers on the substrate; and

forming source and drain regions in the substrate and adjacent to the gate electrode.

2. The semiconductor structure of claim 1 wherein the implanting step includes implanting ions through the gap using a tilted ion beam to produce a halo of implanted ions under the dielectric spacers at the sides of the gap.

3. The semiconductor structure of claim 1, further comprising, prior to forming the gate electrode in the gap, implanting ions through the gap using a normally incident or nearly normally incident ion beam.

4. The semiconductor structure of claim 1 wherein forming the gate electrode comprises:

pre-gate cleaning;

forming a gate dielectric on a bottom of the gap;

forming a second layer of conductive material on the first layer and on the gate dielectric; and

chemical-mechanical polishing to remove the second layer of conductive material from the first layer but not from the bottom of the gap.

5. The semiconductor structure of claim 1, further comprising forming a self-aligned metal silicide contact to the gate and to the source and drain regions.

6. The semiconductor structure of claim 1, wherein the first layer is a series of chemically distinct layers formed by the method comprising:

forming a layer of silicon nitride on the surface of the substrate; and

depositing an oxide layer on the silicon nitride layer, the deposited oxide layer having a thickness in a range of between 100 and 500 nanometers.

7. The semiconductor structure of claim 1, wherein forming an opening through a top one of the series of chemically distinct layers includes reactive ion etching the top one of the series of chemically distinct layers using an anisotropic etch that does not etch a chemically distinct layer beneath the top one of the series of chemically distinct layers.

8. An integrated circuit including field effect transistors formed by a method comprising:

forming a layer of silicon nitride on a substrate;

depositing an oxide layer on the silicon nitride layer, the oxide layer having a first thickness;

forming an opening having a first width through the oxide layer;

forming a blanket dielectric layer having a second thickness on the oxide layer and in the openings, the second thickness being half or less of the first thickness;

removing the blanket dielectric layer from the oxide layer and bottoms of the opening but not from sidewalls of the opening to form dielectric spacers on either side of a gap within the opening, the gap having a second width less than the first width;

forming a gate in the gap;

implanting ions into the substrate at a location beneath the opening, the implanting being performed at multiple angles to provide implanted ions under the dielectric spacers on each side of the opening;

removing the oxide layer and the silicon nitride layer but not the dielectric spacers; and

forming source and drain regions in the substrate.

9. The integrated circuit of claim 8, further comprising, implanting a well in the substrate wherein the step of implanting ions defines opposite sides of a channel formed in the well.

10. The integrated circuit of claim 8, further comprising, prior to forming gates in each of the gaps, implanting ions through the gaps using a normally incident or nearly normally incident ion beam.

11. The integrated circuit of claim 8 wherein forming gates comprises:

pre-gate cleaning;

forming a gate dielectric on bottoms of the gaps;

forming a layer of conductive material on the oxide layer and on the gate dielectric; and

chemical-mechanical polishing to remove the layer of conductive material from the oxide layer.

12. The integrated circuit of claim 8, further comprising forming self-aligned metal silicide contacts to the gates and to the source and drain regions.

13. The integrated circuit of claim 8, wherein forming an opening through the oxide layer includes reactive ion etching the oxide layer using an anisotropic etch that does not etch the silicon nitride layer beneath the oxide layer, where the opening has substantially vertical sidewalls.

14. A semiconductor structure, comprising:

a semiconductor substrate;

a well implanted in the substrate, the well having an opposite conductivity type with respect to the substrate;

first and second dielectric spacers positioned on the substrate and defining opposite sides of an opening;

a gate dielectric positioned on the substrate and in the opening;

a gate electrode formed in the opening and on the gate dielectric, the gate electrode being limited by the dielectric spacers;

first and second halos implanted in the well and under the first and second dielectric spacers, respectively, a channel being defined in the well by the halos; and

source and drain regions implanted in the substrate and adjacent to the first and second halos, respectively.

15. The semiconductor structure of claim 14, further comprising dielectric isolation structures formed in the substrate on opposite sides of the well.

16. The semiconductor structure of claim 14 wherein the first and second halos are formed by ion implanting at plural angles through the opening prior to forming the gate electrode in the opening, the plural angles being sufficient to form the halos only under the dielectric spacers without extending directly under the opening.

17. The semiconductor structure of claim 14 wherein the dielectric spacers have a height that is more than twice a width of the spacers.

18. The semiconductor structure of claim 14, further comprising silicide contacts formed on the gate electrode, source, and drain.

19. The semiconductor structure of claim 14, further comprising:

a first contact coupled to a first one of the source and drain and positioned on a first portion of the gate electrode;

a second contact coupled to a second one of the source and drain; and

a dielectric layer positioned on a second portion of the gate electrode and being defined on opposite sides by the first and second contacts.